

Amendments to the Claims

1. (Currently Amended) A method for correcting a phase of a clock in a data receiver which receives a data flow representing different signal levels with logical high and low signal values and signal transitions positioned therebetween, comprising the steps of:

evaluating the positions of the signal transitions between respective two adjacent logical signal values for correcting the phase of the clock,

wherein the position of a signal transition between a first pair of signal values on a first level, or and a second pair of signal values on a second level is weighted stronger in the evaluation than the positions of signal transitions between adjacent single signal values of different signal levels.

wherein the method comprises the steps of:

a) sampling the data flow with a clock frequency at four intervals adjacent logical signal values, and at a signal transition positioned between the inner intervals for obtaining a position information of the transition relative to the logical signal values;

b) forming sample groups from said signal samples taken in step a).

c) supplying said sample groups to an early-late phase detector which evaluates said sample groups as to whether the phase of said clock frequency is to be shifted, and outputs a control signal for "frequency UP" "frequency DOWN" or "No control value".

d) examining whether there are pairs of logical signal values on the same level with a signal transition between neighbouring pairs, and

e) scaling up said control signal in step c) if the condition under step d) is fulfilled.

2. (Canceled)

3. (Cancelled)